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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 10/689,187
Filing Date: October 20, 2003
Appellant(s): KNALL ET AL.

Pamela J. Squyres
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 22 December 2006 appealing from the Office action mailed 17 April 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The following are the related appeals, interferences, and judicial proceedings known to the examiner which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal:

US Patent Application 10/610,804, which includes an Appeal Brief filed 11 December 2006, was identified by the Appellant as a related appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,835,396	Zhang	11-1998
6,111,302	Zhang et al.	8-2000
4,881,114	Mohsen et al.	11-1989

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

A. Claim 1 stands rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,835,396 to Zhang (hereafter Zhang '396) in view of U.S. Patent No. 6,111,302 to Zhang et al. (hereafter Zhang '302).

Zhang '396 discloses a three dimensional multi-level memory array (figure 1) disposed above a substrate (10), the array comprising: a first plurality of spaced apart rail stacks (bottom electrode 503 + TiW barrier layer disposed thereon for figs. 5-6, or alternately, layers 503 and 502cb in figures 10a,b) disposed at a first height in a first direction above the substrate (see figure 6A and figure 1); a second plurality of rail stacks (top electrode 501+ TiW barrier layer disposed thereon, or alternately, layers 501 and 502ca in figures 10a,b) disposed above the first height and in a second direction different from the first direction (figures 1 and 6A) and a plurality of memory cells (formed from

501, 502, and 503 at the relative intersections of 501 and 503), each memory cell comprising an antifuse (502; see column 7, lines 10-18; also see column 6, lines 18-35, noting that thin layers of intrinsic amorphous silicon act as an antifuse), wherein the antifuses are disposed at the intersections of the rail stacks (see figure 6A).

Zhang '396 fails to specify that silicon nitride could be used as the metal-to-metal antifuse material.

Zhang '302 teaches that silicon nitride is an appropriate material for use as a metal-to-metal antifuse, and that it may be used interchangeably with other known antifuse materials, such as amorphous silicon (see column 3, lines 39-56).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the amorphous silicon antifuse layer of Zhang '396, such that it is silicon nitride, as suggested by Zhang '302. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use silicon nitride for the metal-to-metal antifuse, because Zhang '302 shows that both silicon nitride and amorphous silicon are considered art recognized equivalents that may be used interchangeably as metal-to-metal antifuses (Zhang '302 – column 3, lines 39-56), and that both materials provide the advantages of eliminating switch-off phenomena and improving the on and off-state properties of the antifuse (see Zhang '302, column 2, lines 14-33). A person skilled in the art would further appreciate that since both Zhang '302 and Zhang '396 are directed toward metal-to-metal antifuses using generally similar materials and similar structures, it would be reasonable and apparent to apply any of the specific antifuse materials in Zhang '302 to the structure of Zhang '396. It has been held

that "the selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in Sinclair & Carroll Co. v. Interchemical Corp., 325 U.S. 327, 65 USPQ 297 (1945). "Reading a list and selecting a known compound to meet known requirements is no more ingenious than selecting the last piece to put in the last opening in a jig-saw puzzle." 325 U.S. at 335, 65 USPQ at 301).

B. Claims 1 and 2 stand rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,835,396 to Zhang in view of U.S. Patent No. 4,881,114 to Mohsen et al.

Regarding claim 1, Zhang discloses a three dimensional multi-level memory array (figure 1) disposed above a substrate (10), the array comprising: a first plurality of spaced-apart rail stacks (see figure 10a, formed from layers 503 and 502cb) disposed at a first height in a first direction above the substrate (see figures 1 and 10a; column 10, lines 7-12, noting that layers 503 and 502cb are patterned together in a rail shape); a second plurality of spaced apart rail stacks (formed from layers 502ca and 501); a plurality of memory cells (formed from 501,502ca,502cc,502cb and 503 at the intersection of the first and second rails; also see figures 1, 7, and 12), each memory cell comprising an antifuse (502ca), wherein the antifuses are disposed at the intersections of the first and second rail stacks (antifuses are disposed on the bottom of and across the entire extent of the second rail stack, and thus, are present at the intersection of the two rail stacks – see figure 10A).

Zhang fails to disclose that the antifuse is formed of silicon nitride.

Mohsen discloses a memory cell having a silicon nitride antifuse (14; see column 4, lines 22-25) disposed between layers comprising either metal or semiconductor materials (column 4, lines 4-10).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the antifuse of Zhang, such that it is formed of silicon nitride, as taught by Mohsen. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use silicon nitride as the antifuse, because Mohsen shows that silicon nitride is an appropriate antifuse for use between metal electrodes or metal and semiconductor electrodes (Mohsen, column 4, lines 4-10), and that silicon nitride used as an antifuse has the advantageous properties of high reliability in the programmed and unprogrammed state, controllable antifuse rupturing properties, and high conductivity after programming (see Mohsen, column 2, lines 29-40).

Regarding claim 2, Zhang discloses that the array comprises polysilicon pn diodes (column 6, lines 50-55), and that it is desirable for the quasi-conduction layer (which is formed by the polysilicon pn diodes) to have the characteristic of having a low resistance current path when subjected to a sufficiently high forward bias, a high resistance path when subjected to a low forward bias or a reverse bias (column 6, lines 8-17; also see figure 8), and as large as possible of a nonlinear IV response in order to improve storage capacity (see column 6, lines 50-62 and column 8, line 55- column 9, line 7).

Zhang is silent as to the doping levels in the pn junction diode.

Mohsen suggests that the diode is formed from a heavily doped layer adjoining a moderately doped opposite conductivity layer (column 3, lines 45-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify that the doping levels of the pn junction diode of Zhang are consistent with a p+n or p-n+ device, as suggested by Mohsen. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use a pn diode with one highly doped side (i.e. p+n) because it is well established in the semiconductor device arts that such a device will have increased current flow for each bias level, which appropriately corresponds to the conditions disclosed by Zhang as most desirable, and would result in a lower resistance current path for forward bias, generally insignificant changes to the reverse bias characteristic, and greater nonlinearity of the IV response, as is appreciated by a person having skill in the art. It is expected that even lacking knowledge of the properties of p+n diodes, Zhang would arrive at a p+n structure through routine optimization of the doping levels for the diode to achieve the properties listed supra. Since Mohsen further indicates that a p+n diode portion is compatible with anti-fuse type memory cells and can function to drive and direct the current through the antifuse memory cell, a person skilled in the art would further conclude that it would be reasonable to select a p+n diode for a memory cell diode structure. Although Zhang is silent as to the specific doping levels, it has been held that "where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (1955).

(10) Response to Argument

A. Regarding the combination of Zhang '396 and Zhang '302:

The Appellant first argues that the purpose of Zhang '302 is to prevent switch off (see Appeal Brief, page 7, lines 7-8), and that the switch-off phenomenon in Zhang '302 is caused by use of high thermal resistance materials for the conductors (Appeal Brief, page 7, third full paragraph). The Appellant then notes that Zhang '396 does not teach conductors formed of high thermal resistance materials (Appeal Brief, paragraph bridging pages 7-8).

In response, the Examiner concedes that the use of amorphous silicon or silicon nitride as an antifuse material will only eliminate switch-off phenomena when accompanied by the low thermal resistance conductor as in Zhang '302. However, the Examiner maintains that since the claims require neither the use of a low thermal conductivity material nor the elimination of switch-off, the Appellant's arguments about the purpose of the Zhang '302 invention or about the lack of low thermal conductivity layers in Zhang '396 are moot.

The Appellant further argues that Zhang '302 and Zhang '396 do not have similar materials and structures, since Zhang '302 requires the use of high thermal resistance conductors (see Appeal Brief, page 7, last paragraph – page 8, first paragraph) which are not present in Zhang '396, and since Zhang '396 uses layers between the conductors in addition to the antifuse layer. The Appellant indicates that it would not be reasonable to combine the antifuse material from Zhang '302 with the structure in Zhang '396 since different materials and layers are present.

In response to these arguments, the Examiner notes that Zhang '396 directly states that the embodiments of figures 6B-6E (recited in the rejection) have a structure similar to a conventional metal–to-metal antifuse (see Zhang '396, column 7, lines 10-18). Hence, the Examiner considers it reasonable to compare the Zhang '396 structure with the metal-to-metal antifuse in Zhang '302. The Examiner further notes that both Zhang '302 and Zhang '396 include a bottom electrode, an antifuse layer stacked thereon, and a top electrode, with optional barrier layers disposed on each electrode (see Zhang '396, column 6, lines 17-35 and column 9, lines 26-40; also see Zhang '302, column 3, lines 39-45). It is noted that despite the Appellant's argument that figures 5a-6e in Zhang '396 teach an MPROM embodiment that does not include an antifuse, Zhang '396 specifically identifies quasi-conduction layer '502 as a thin amorphous silicon layer or ceramic oxide layer (Zhang '396, column 6, lines 17-35), and later states that thin amorphous silicon layers or ceramic oxide layers function as antifuses (Zhang, column 9, lines 26-40). Thus, the Examiner maintains that Zhang '396 and '302 are considered to have similar materials and similar structures, and thus be reasonably combined.

The Examiner maintains, however, that use of different materials and layers for the Zhang '396 and Zhang '302 references does not render the combination of the references unreasonable, particularly since the language of claim 1 neither requires nor prohibits the presence of additional layers in the memory cell structure. The only conditions that must be met to establish a prima facie case of obviousness are that the prior art references much teach all of the claim limitations, there must be some suggestion or motivation to combine the references, and there must be a reasonable expectation of success (see MPEP § 2143). Even if the embodiments in figures 9a-9c of Zhang '396, involving the use of an additional layer abutting

the antifuse layer, are applied in the obviousness rejection, the Examiner maintains that the teaching in Zhang '302 pertaining to the general art-recognized equivalence between the use of amorphous silicon, silicon nitride, or a number of other common antifuse materials (Zhang '302, column 3, lines 39-50) is sufficient for maintaining a prima facie obviousness determination, particularly in view of the lack of criticality of such an element as set forth in the specification of the present application (see paragraph 0029 of the specification of the present application, noting that line 11 of paragraph 0029 provides the only citation in the specification of silicon nitride as an antifuse material).

The Appellant summarizes the previously set forth arguments (see Appeal Brief, page 9, first full paragraph) that the Zhang '302 and Zhang '396 structures are not similar and that Zhang '302 is drawn toward preventing switch-off, which is inapplicable to the Zhang '396 invention.

In response, the Examiner maintains that the Zhang '302 and '396 structures are sufficiently similar, and that the question of switch-off is moot, as the claim language does not limit the structure in such a manner. Since Zhang '302 specifically teaches that SiN is a suitable material known and used in the art as a metal-to-metal antifuse, has the resistance properties required by Zhang '396 (and implicit to the term "antifuse"), and is usable interchangeably with other antifuse materials, such as the amorphous silicon used in Zhang '396, and since the specification of the present application does not particularly point out the criticality of the use of silicon nitride, but rather equates the use of silicon nitride with undoped silicon, silicon oxide, silicon oxynitride, or other thin insulating layers (see specification of the present application, paragraph 0029) in a manner similar to that in Zhang '302 (see Zhang '302, column 3, lines 39-45), the Examiner maintains that it is highly reasonable to substitute the silicon nitride antifuse

for the amorphous silicon antifuse, based on the principles of art recognized equivalence and art-recognized suitability as set forth in the rejection supra.

B. Regarding the combination of Zhang '396 and Mohsen:

The Appellant argues that the Mohsen passage at column 4, lines 4-10 should reasonably be interpreted as requiring formation of a diode only when the antifuse is ruptured, due to the diode portions being disposed on opposite sides of the antifuse layer (see Appeal Brief, pages 10-11). Since Zhang '396 only teaches embodiments wherein the diode is completely formed on one side or the other of the antifuse, and not wherein the diode portions are separated by the antifuse, the Appellant asserts that the combination of Zhang '396 and Mohsen, wherein the silicon nitride antifuse material of Mohsen replaces the antifuse layer of Zhang '396, is not reasonable.

In response, the Examiner notes that the cited passage in Mohsen *does* explicitly state that the silicon nitride antifuse may be positioned between any of the doped polysilicon, the doped single crystal silicon, or metal or a combination of the above. In the Examiner's view, it is not reasonable to interpret Mohsen in a manner contradicting what is expressly stated in Mohsen. However, even if Mohsen is interpreted such that the antifuse is sandwiched between polysilicon layers or between a polysilicon layer and a metal layer, thus forming a pn diode or Schottky diode upon rupture, the Examiner maintains that the combination of Zhang '396 and Mohsen meets the criteria for a 35 U.S.C. 103 rejection. Mohsen provides motivation for using a silicon nitride structure by citing low programming currents and higher operational speeds, as is well known in the art (also see Mohsen, column 7, lines 34-50). Thus, one skilled in the art

would reasonably expect that a silicon nitride antifuse when applied to the structure of Zhang '396 would achieve similar benefits. The Examiner maintains that the structural differences recited by the Appellant are moot, since the position of the pn diode portions that determine whether a diode is present before or only after antifuse rupture do not appear in the claims, and since exact similarity between the diode structure of Zhang '396 and the diode structure of Mohsen is not required to maintain a prima facie case of obviousness, providing that the motivation to combine the references is present.

Regarding both the Zhang '396 in view of Zhang '302 and Zhang '396 in view of Mohsen rejections:

The Examiner notes that in the Appeal Brief for Application serial number 10/610,804, identified by the Appellant as a related appeal in section II, Related Appeals and Interferences, the Appellant concedes the following:

> The Examiner is correct that it is known to use silicon nitride as an antifuse material, and that a silicon nitride antifuse will, in general, rupture faster than a comparable dielectric rupture antifuse formed of other material, such as amorphous silicon or silicon dioxide (see Appeal Brief for SN 10/610,804, page 8, last paragraph).

The Examiner maintains that substitution of a silicon nitride antifuse material for the antifuse material in the structure in Zhang '396, based on any of the teachings of Zhang '302, Mohsen, or the Appellant's admission is simply a substitution of a known antifuse material into a known antifuse memory structure to achieve an effect consistent with that which is already well known in the art.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Jennifer M. Dolan
Examiner
Art Unit 2813

JMD
21 March 2007

Conferees:

David Blum

Carl Whitehead, Jr.